

REMARKS

Applicant respectfully traverses and requests reconsideration.

Claims 1-6, 10-13 and 23-27 stand rejected under 35 U.S.C. §102(e) as being anticipated by Apostol, Jr. et al. (U.S. Patent No. 6,247,084). Apostol is directed to an integrated circuit with a unified memory system and dual bus architecture but does not appear to be directed to a flat panel display monitoring method or apparatus as claimed. As to claim 1, the office action cites column 6, lines 1-65 and column 30, line 47 through column 31, line 65 as allegedly teaching a method for detecting a monitor wherein the method comprises monitoring one pin of a connector coupled to a flat panel display. However, Applicant respectfully submits that the cited portion does not teach what is alleged. Instead, the cited portion appears to merely indicate that there are display pins as part of the integrated circuit 10 which are coupled to an LCD display. Applicant is unable to find any mention of a circuit or any other structure in the cited portion that monitors one pin of a connector coupled to a flat panel display. In addition, as to claim 1, the office action alleges that the cited reference teaches asserting an output signal to indicate the one pin is in a first state. However, there is no cited portion of the reference that is designated as allegedly teaching this subject matter. Also, Applicant is unable to find such teaching. As such, the claim is also in condition for allowance for this reason as well.

The office action also cites column 5, line 45 through column 7, line 40 and column 30, line 47 to column 31, line 65 as allegedly teaching receiving the output signal at a first display engine wherein the output signal has been asserted to indicate that the one pin is in a first state. However, Applicant is unable to locate such a teaching. The cited portions merely state that the integrated circuit 10 includes display pins. If the rejection is maintained, Applicant respectfully requests a showing as to where the cited reference teaches the claimed subject matter as

Applicant is unable to find the alleged teachings. Accordingly, claim 1 is in condition for allowance.

The dependent claims add additional novel and non-obvious subject matter.

As to claim 23, Applicant respectfully reasserts the relevant remarks made above with respect to claim 1 and as such, this claim is also believed to be in condition for allowance.

As to claim 25, the office action has alleged that, among other things, the cited reference teaches asserting an output signal to indicate that a pin of a connector coupled to a flat panel display is in a first state and providing an interrupt signal in response to the asserted output signal in column 6, lines 1-65, column 9, line 39 through column 21, line 25. However, the portion of column 6 appears to merely refer to the overall system architecture shown in FIG. 4 and does not describe any monitoring of a pin of a connector and asserting an output signal to indicate that the pin is in a first state nor providing an interrupt signal in response to the asserted output signal. In addition, columns 19-21 refer to the inbound data transfers, the processor 12, the memory controller 14, and bus arbiter signals, but does not teach the subject matter as alleged. If the rejection is maintained, Applicant respectfully requests a showing as to where the reference teaches the claimed subject matter as Applicant is unable to find such teachings. Accordingly, the claims are in condition for allowance.

Applicant respectfully submits that the claims are in condition for allowance and that a timely Notice of Allowance be issued in this case. The Examiner is invited to contact the below-listed attorney if the Examiner believes that a telephone conference will advance the prosecution of this application.

Respectfully submitted,

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By: Christopher J. Reckamp
Christopher J. Reckamp
Registration No. 34,414

Vedder, Price, Kaufman & Kammholz, P.C.
222 N. LaSalle Street
Chicago, IL 60601
(312) 609-7500
FAX: (312) 609-5005